WHAT IS CLAIMED IS:

Sub a1

1. A data processing device comprising:

an instruction decoder for sequentially decoding a plurality of instructions described in a program sequence and outputting a control signal respectively corresponding to the instructions, and

an instruction execution unit for executing operations respectively designated by said plurality of instructions in accordance with said control signal outputted from said instruction decoder, wherein

said instruction decoder decodes a first instruction among said plurality of instructions and outputs a first control signal in a first period;

said instruction execution unit executes the operation designated by said first instruction in accordance with said first control signal in a second period succeeding to said first period;

said instruction decoder outputs a second control signal by decoding a second instruction of which operation is executed under a predetermined condition among said plurality of instructions in a third period; and

said instruction execution unit judges whether or not said predetermined condition is satisfied and executes the operation designated by said second instruction in response to a result of the judgement in a fourth period which is started after elapsing the same

time as said second period or longer from the ending of said third period.

2. A data processing device according to Claim 1 further comprising:

a register for designating amount of delay which can variably set a value to be held therein, wherein,

said instruction execution unit starts the judgement of whether or not said second operation instruction satisfies the predetermined condition in response to the value held in the register for designating amount of delay as an amount of delay.

3. A data processing device according to Claim 2, wherein

said second instruction has a field for designating operation and a field for designating amount of delay, which designates an interval between the ending of said third period and the starting of said fourth period; and

the amount of delay is set in the register for designating amount of delay in accordance with a content described in said field for designating amount of delay.

4. A data processing device according to Claim 2 further comprising:

a program counter for sequentially counting addresses respectively corresponding to the plurality of instructions and holding the addresses, wherein

said register for designating amount of delay hold an address value to designate the amount of delay; and

the instruction execution unit starts the judgement of whether or not said second instruction satisfies the predetermined condition in response to an event that the address value held in said register for designating amount of delay is in agreement with a value of the program counter.

Sub a2 > 5. A data processing device according to Claim 1, wherein

the instruction execution unit judges whether or not the predetermined condition is satisfied in a fifth period included in said fourth period and executes the operation designated by said second instruction when said predetermined condition is satisfied in a sixth period which is included in said fourth period and starts after elapsing the same time as said second period or longer from the ending of said fifth period.

6. A data processing device according to Claim 5 further comprising:

a first register for designating amount of delay and a second register for designating amount of delay both of which can variably set values to be held respectively therein, wherein

said instruction execution unit starts the judgement of whether or not said second instruction satisfies the predetermined condition in accordance with a value held in said first register for designating amount of delay as an amount of a first delay and starts to execute the

operation designated by said second instruction when the predetermined condition of said second instruction is satisfied in accordance with a value held in said second register for designating amount of delay as an amount of a second delay.

7. A data processing device according to Claim 6, wherein

said second instruction has a field for designating operation, a field for designating amount of first delay which designates a time between the ending of said third period and the starting of said fourth period and a field for designating amount of second delay which designates a time between the ending of said fifth period and the starting of said sixth period; and

the amount of said first delay is set in said first register for designating amount of delay in accordance with a content described in said field for designating amount of first delay and the amount of said second delay is set in said second register for designating amount of delay in accordance with a content described in said field for designating amount of said second delay.

8. A data processing device according to Claim 6 further comprising:

a program counter which sequentially counts addresses respectively corresponding to the plurality of instructions and holds the addresses, wherein

said first register for designating amount of delay and said second register for designating amount of delay hold address values respectively as the amount of said first delay and the amount of said second delay;

said instruction execution unit starts to judge whether or not the predetermined condition is satisfied in response to an event that the address value held in said first register for designating amount of delay is in agreement with a value of the program counter and starts to execute the operation designated by the second operation instruction when the predetermined condition is satisfied in response to an event that the address value held in said second register for designating amount of delay is in agreement with the value of the program counter.

9. A data processing device according to Claim 1, wherein

the instruction decoder decodes a third instruction among the plurality of instructions in a seventh period which is started after said third period, in order to output a third control signal;

the instruction execution unit executes an operation designated by said third instruction in accordance with said third control signal and writes a result of the operation in a predetermined memory location in an eighth period which is started after said seventh period;

said second instruction designates an operation to be executed in a case that the operation result of said third operation instruction has a predetermined value; and

said instruction execution unit determines whether or not the operation designated by said second instruction is executed in reference of the predetermined memory location so that the starting of said fourth period is at least later than said eighth period.

10. A data processing device according to Claim 9, wherein

the predetermined memory location is a flag or a register; and

said third instruction is a comparison instruction which compares values of two registers and writes a result of the comparison in the predetermined memory location.

11. A data processing device according to Claim 1, wherein

the second operation instruction is a branch instruction, a jump instruction or an add instruction.

12. A data processing device according to Claim 1, wherein

each of the plurality of instructions has a field for designating an operation which designate contents of the operation, a field for designating a condition which

designates an execution condition of the operation and a field for designating amount of delay which designates an amount by which timing for judging the execution conditions is delayed;

said first instruction is an instruction that is unconditionally executed and a description indicating an unconditionality is described in said field for designating the condition of said first instruction;

a description indicating a condition and a description indicating an interval between the ending of said third period and the starting of said fourth period are described respectively in said fields for designating the condition and the amount of delay of said second instruction;

the instruction decoder outputs the first control signal in accordance with said field for designating the operation of said first instruction and controls the instruction execution unit so that the instruction execution unit executes unconditionally the operation designated by said first instruction in said second period based on said field for designating the condition of said first instruction; and

the instruction decoder outputs said second control signal in accordance with said field for designating the operation of said second instruction, controls the instruction execution unit so as to judge whether or not the condition is satisfied in said fourth period in

accordance with said field for designating the amount of delay and controls the instruction execution unit so as to determine whether or not the condition is satisfied in accordance with said field for designating the condition of said second instruction.

13. A data processing device according to Claim 1, wherein each of the plurality of instructions has a field for designating an operation which designates the contents of the operation, a field for designating a condition which designates the execution condition of the operation and a field for designating an amount of delay which designates the amount by which timing for judging the execution condition is delayed;

said first instruction is a conditional instruction;

a description indicating a first condition different from a second condition which is the predetermined condition of said second instruction is described in said field for designating the condition and a description indicating that said first condition should be judged in said first period is described in said field for designating the amount of delay respectively of said first instruction;

a description indicating said second condition is described in said field for designating the condition and a description indicating the interval between the ending of said third period and the starting of said fourth period is described in said field for designating

the amount of delay respectively of said second instruction;

the instruction decoder outputs said first control signal in accordance with said field for designating the operation of said first instruction and controls said instruction execution unit so as to execute the operation designated by said first instruction based on said field for designating the condition and said field for designating the amount of delay of said first instruction in said second period;

said instruction decoder outputs said second control signal in accordance with the field for designating the operation of said second instruction, controls said instruction execution unit so as to judge whether or not said second condition is satisfied in accordance with said field for designating the amount of delay of second instruction in said fourth period, and controls said instruction execution unit so as to determine whether or not said second condition is satisfied in accordance with said field for the condition of said second instruction.

Sub a3

14. A data processing device comprising:

an instruction decoder which sequentially decodes a plurality of instructions described in a program sequence and outputs a control signal corresponding to each instruction, and

an instruction execution unit which executes

operations designated by the plurality of instructions in accordance with the control signals outputted from said instruction decoder, wherein

when one of said plurality of instructions is a conditional instruction, said instruction decoder outputs a first control signal by decoding said conditional instruction;

said instruction execution unit includes a first register for holding said first control signal outputted from said instruction decoder, a second register for holding a first description indicating a condition under which an operation designated by the conditional instruction is executed and a third register for holding a second description indicating a time for starting a judgement of said condition; and

said instruction execution unit starts to judge whether or not said condition is satisfied based on said first description held in said second register in response to an event that the time for starting the judgement of the condition is detected based on said second description held in said third register and reads said first control signal held in said first register in response to the result of the judgement, and starts to execute the operation designated by said conditional instruction in accordance with said first control signal.

15. A data processing device according to Claim 14,

wherein

said second description held in said third register can be variably set.

16. A data processing device according to Claim 14, further comprising:

a program counter which sequentially counts an address corresponding to each of the plurality of instructions and holds the address, wherein an address value is held in said third register as said second description; and

said instruction execution unit, detects an event that the address value held in said third register is in agreement with an address of said program counter and starts to judge whether or not said condition is satisfied in response to the detection.

17. A data processing device according to Claim 15, wherein

said conditional instruction has a field for designating an operation which designate contents of the operation, a field for designating condition which designates the executing condition of the operation and a field for designating an amount of delay which designate a time for judging the execution condition;

said instruction decoder produces said first control signal based on contents described in said field for designating operation, outputs the contents described in said field for designating the condition as said first

description and outputs the contents described in said field for designating the amount of delay;

said first description outputted from said instruction decoder is held in said second register; and

said instruction execution unit writes said second description in said third register in accordance with said field for designating the amount of delay outputted from said instruction decoder.

18. A data processing device according to Claim 14, wherein

the instruction execution unit further has a fourth register for holding a third description indicating a time for starting the operation designated by the instruction; and

said instruction execution unit detects the time for starting the operation designated by the instruction, judges whether or not the condition is satisfied in response to a result of the detection and starts the operation designated by the instruction in response to a result of the judgement, in accordance with said third description.

19. A data processing device according to Claim 18, further comprising;

a program counter for sequentially counting an address corresponding to each of the plurality of instructions and holds the address, wherein

an address value is held in said third register as

said second description;

an address value which is different from said second description is held in said fourth register as said third description;

said instruction execution unit detects an event that the address value held in said third register is in agreement with an address of said program counter, starts to judge whether or not the condition is satisfied in response to the detection, detects an event that the address value held in said fourth register is in agreement with the address of said program counter and starts to execute the operation designated by said instruction in response to the detection.

20. A data processing device according to Claim 18, wherein

said conditional instruction has a field for designating an operation which designate contents of the operation, a field for designating a condition for designating an execution condition of the operation, a field for designating an amount of a first delay which designates a time for judging the execution condition and a field for designating an amount of a second delay which designates a time for starting the execution of the operation;

said instruction decoder produces said first control signal based on the contents described in said field for designating an operation, outputs the contents described

in said field for designating a condition as said first description, and outputs the contents described in said field for designating an amount of said first delay and said field for designating an amount of said second delay; and

said instruction execution unit writes said second description in said third register in accordance with the contents described in said field for designating the amount of said first delay outputted from said instruction decoder and further writes said third description in said fourth register in accordance with the contents described in said field for designating the amount of said second delay outputted from said instruction decoder.

add
af